AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

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1. (Currently Amended) A semiconductor device, comprising

an I/O region formed on a chip and having at least an input/output pad;

a plurality of active ~~region~~ regions formed on said chip, said active regions being separated from one another by a boundary region;

a plurality of logic circuits having either one of the same functions and different functions being mounted in each of said active regions, and

a selection circuit for selectively operating only one of said plurality of mounted logic circuits;

wherein each of said plurality of mounted logic circuits is operated by setting an SEL signal for turning on/off a transistor for each of said mounted logic circuits, to one of a high and a low level.

2. (Previously Amended) The semiconductor device comprising:

an I/O region formed on a chip and having at least an input/output pad;

an active region formed on said chip;

a plurality of logic circuits having either one of the same functions and different functions being mounted in said active region, and

a selection circuit for selectively operating only one of said plurality of mounted logic circuits;

wherein said selection circuit includes a disconnecting section, and

said disconnecting section is disconnected to allow permanent setting of an operable circuit.

3. (Original) The semiconductor device according to claim 2, wherein said disconnecting section includes a fuse.

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4. (Previously Amended) The semiconductor device according to claim 1, wherein said selection circuit selects a logic circuit to be operated on a basis of a signal input supplied from an outside through said input/output pad.

5. (Previously Amended) The semiconductor device comprising:

an I/O region formed on a chip and having at least an input/output pad;

an active region formed on said chip;

a plurality of logic circuits having either one of the same functions and different functions being mounted in said active region, and

a selection circuit for selectively operating only one of said plurality of mounted logic circuits;

wherein said selection circuit includes a transistor element connected in series with each said logic circuit between said logic circuit and a power terminal, and

said transistor element selects a logic circuit to be operated on a basis of a signal input supplied from an outside through said input/output pad.